THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 42

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YOSHIMITSU INAMORI
and KOICHI ODA

Appeal No. 1996-2369
Application No. 08/191,723[1]

HEARD: October 21, 1999

Before JERRY SMITH, FLEMING, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1, 3, and 5-8. The appellants filed a first amendment after final rejection on

---

[1] The application was filed on February 4, 1994. It is a continuation of Application Serial No. 07/743,608, which was filed on August 9, 1991 and is now abandoned.

March 14, 1995, which was denied entry. The appellants filed a second amendment after final rejection on June 15, 1995, which was entered. We reverse.

BACKGROUND

The invention at issue in this appeal relates to a liquid crystal display (LCD). The LCD has an effective horizontal address range of -1024 to +1023. Only eleven bits of the sixteen bits of LCD's address data are needed to specify the effective horizontal address range. The other five bits, which are unused, can be a source of error. Specifically, address data in the five bits can cause an unintentional display on the LCD. In the past, software was used to discriminate address data in the five bits to prevent unintentional display. The software burdened the central processing unit (CPU) and slowed the display. The appellants' invention employs hardware circuitry to reduce the burden and speed the display.

Also in the past, when write instructions were to be successively executed over a range of addresses in the LCD, it was necessary to designate write addresses for each address.

In addition, data stored in the CPU's result buffer had to be temporarily stored elsewhere and, upon executing the next write instruction, retrieved for transfer to the LCD's segment-drive circuit. Such processing burdened the CPU. Successive execution of read instructions produced a similar problem. The appellants' invention employs a loop count register to reduce the burden and speed the display.

Claim 1, which is representative for our purposes, follows:

> 1. A display control circuit which causes display to be performed on a display means having a display space in which addresses are set, by supplying to the display means address data of a first number of bits corresponding to the display capacity of the display space, comprising:
>
> data regulating means which receive the address data of the first number of bits and which output address data of a second number of regulated bits comprising the first number of bits which have been logically combined with a predetermined number of extended bits, wherein when the address data of the first number of bits are incorrect and are for a display position outside the addresses in the display space but which when unregulated may result in an undesired display within the display space, said data regulating means causing the address data of the second number of regulated bits to be within an addressing range outside the display space based on the address data provided by said second number of regulated bits, and

> outside-address detecting means for detecting the address data of the first number of bits when the address data of the first number of bits is outside the addresses in the display space,
>
> whereby the supply of incorrect address data to the display means is prevented from causing said undesirable display to be performed within said display space.

Claim 1 stands rejected under 35 U.S.C. § 112 as indefinite. Claims 1, 3, and 5-8 also stand rejected under 35 U.S.C. § 103 as obvious over the appellants' admitted prior art. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejections and evidence advanced by the examiner. Furthermore, we duly considered the arguments of the appellants and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claim 1 as indefinite. We are also persuaded that the examiner erred in rejecting claims 1, 3, and 5-8 as obvious. Accordingly, we reverse. Our opinion

addresses the definiteness of claim 1 and the nonobviousness of claims 1, 3, and 5-8.

Definiteness of Claim 1

Regarding claim 1, the examiner alleges, “it is not clear that the address data of the first number of bits are outside of the display ... and the address data of the second number of bits are also outside of the display space.” (Examiner’s Answer at 3.) The appellants offer the following response.

> [T]he "data regulating means" clause clearly specifies that regulation is required where the first number of address data bits is incorrect and is for a display position outside the addresses in the display space, but which when unregulated may result in an undesired display within the display space, the first number of bits is logically combined with a predetermined number of extended bits to positively cause the regulated bits of the address data to be within an addressing range outside the display space. (Appeal Br. at 10.)

We agree with the appellants.

The test for the definiteness of a claim is whether one skilled in the art would understand the bounds of the claim when read in light of the specification. If the claim read in light of the specification would reasonably apprise one so

skilled of the scope of the invention, 35 U.S.C. § 112 demands no more. Miles Labs., Inc. v. Shandon Inc., 997 F.2d 870, 875, 27 USPQ2d 1123, 1126 (Fed. Cir. 1993). Here, when read in light of the specification, one skilled in the art would understand the following features of the appellants' invention. The claimed "address data of the first number of bits" could specify a display position that is outside the LCD's effective address area 59. Without correction, this specification may result in an undesired display within the effective address area. Fig. 1, (0,0). The invention corrects the bits of the address data to be within the extension address area 11 of the LCD 11, which is outside the effective address area.

In summary, one skilled in the art would understand the bounds of the claim 1 when read in light of the specification. We demand no more. Therefore, we reverse the rejection of claim 1 under 35 U.S.C. § 112. Next, we address the nonobviousness of claims 1, 3, and 5-8.

Nonobviousness of Claims 1, 3, and 5-8

We begin our consideration of the nonobviousness of claims 1, 3, and 5-8, by noting three principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). (1) In rejecting claims under § 103, the patent examiner bears the initial burden of establishing a prima facie case of obviousness. (2) A prima facie case is established when teachings from the prior art would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. (3) If the examiner fails to establish a prima facie case, an obviousness rejection will be reversed. With these in mind, we analyze the appellants' arguments.

Regarding claims 1 and 5-7, the appellants begin by arguing that "the description of Figures 1 through 3 and the present disclosure at most merely mention address bits and do not imply or remotely suggest the existence of a predetermined number of extended bits or logically combining such extended bits with the address bits." (Appeal Br. at 17.) They add, "merely because an address data is [sic] 'discriminated', it does not follow that the erroneous

address data is [sic] ‘corrected’.” (Id.) The appellants conclude their argument as follows.

> [T]he Examiner has failed to provide any reasonable basis as to why the artisan would have found it obvious to modify that which is acknowledged to be prior art in Figures 1 through 3 in such a manner as to arrive at that which is required in claim 1 including a "data regulating means" and a "detecting means" .... (Appeal Br. at 18.)

The examiner replies, “the difference between Appellant's device and the prior art is software and hardware. One can combine two address data bits by hardware as Appellant can, the software of prior art (figures 1-3) can do the same function combining two address data bits as Appellant's device.” (Examiner’s Answer at 12.) We agree with the appellants.

Independent claim 1 specifies in pertinent part the following limitations:

> data regulating means which receive the address data of the first number of bits and which output address data of a second number of regulated bits comprising the first number of bits which have been logically combined with a predetermined number of extended bits, wherein when the address data of the first number of bits are incorrect and are for a display position outside the addresses in the

> display space but which when unregulated may result in an undesired display within the display space, said data regulating means causing the address data of the second number of regulated bits to be within an addressing range outside the display space based on the address data provided by said second number of regulated bits ....

Giving the claim its broadest reasonable interpretation, the limitations recite a data regulating means for logically combining address data with a predetermined number of extended bits.

The examiner fails to show a teaching or suggestion of this limitation in the prior art. He admits that the appellants' admitted prior art "does not expressly details [sic] the first determined number of bits logically combined with a predetermined numbers [sic] of extended bits ...." (Examiner's Answer at 5.) Nevertheless, the examiner concludes that it would have been obvious to logically combine "two predetermined number of bits ... because the address data input are corrected as taught by Applicant's [sic] admitted prior art." (Id.)

We note that the appellants' admitted prior art merely teaches that "address data not within the scope of effective address are discriminated ... so that no undesired display can occur within the effective display space." (Spec. at 4.) Neither the use of extended bits nor the conversion of address data is disclosed therein. Consequently, the admitted prior art neither teaches nor would have suggested the data regulating means as claimed.

Regarding claim 3, the appellants argue, "As to that which is allegedly disclosed by the admitted prior art, there is clearly no disclosure of a loop count register means as claimed." (Appeal Br. at 18.) They add, "Moreover, in the description of a block transfer such as a write loop beginning with the last line at page *6* of the present disclosure, it is believed to be abundantly clear that no loop count register means is included." (Id. at 18-19.) The examiner replies, "Claim 3 simply requires a loop counter means for storing operation number data input from the control means. This broadly reads on the result buffer (112) for storing the

display data from CPU (107) and arithmetic (111)."

(Examiner's Answer at 12.) We agree with the appellants.

The examiner errs in interpreting the scope of claim 3. The claim 3 recites more that "a loop counter means for storing operation number data input from the control means." (Examiner's Answer at 12.) Independent claim 3 specifies in pertinent part the following limitations:

> a loop count register means for storing operation number data input from the control means, said operating number data being the number of repeated logical operations to be sequentially performed by said column drive means, and display control data memory means responsive to said operating means and said loop count register means for storing display control data for updating the display address of the display data representing the result of said logical operations.

Giving the claim its broadest reasonable interpretation, the limitations recite a loop count register for storing a count of the number of times a repeated logical operation is to be sequentially done by a column drive means.

The examiner fails to show a teaching or suggestion of these limitations in the prior art. As aforementioned, the

examiner reads the loop counter register of the claim on the result buffer 112 of the appellants' admitted prior art. The result buffer, however, merely stores results of arithmetic operations performed by the arithmetic circuit 111 of the appellants' admitted prior art. (Spec. at 7.) Consequently, the result buffer neither teaches nor would have suggested a loop count register means for storing a count of the number of times a repeated logical operation is to be sequentially done by a column drive means.

Regarding claim 8, the appellants argue, "At best, the portion bridging pages 3 and 4 of the present specification merely indicate that bad or incorrect addresses are detected and ignored or not used as opposed to being converted to an address by a hardware conversion means in the particular manner specified in the claim." (Appeal Br. at 14.) The examiner replies, "The term 'discriminate' does not imply that the address data must be destroyed or not be used as argued by Appellant." (Examiner's Answer at 10.) We agree with the appellants.

Independent claim 8 specifies in pertinent part the following limitations:

> hardware conversion means responsive to said address data bits and said means for detecting for logically converting said address data bits to new address data bits within an extended addressing range beyond said maximum effective display space so as to prevent the occurrence of the undesired display at an addressable position within said maximum effective display space of the display means,
>
> said hardware conversion means including logic circuit means for producing and logically combining a predetermined number of extended address data bits with said received address data bits for producing said new address data bits.

Giving the claim its broadest reasonable interpretation, the limitations recite a logic circuit means for producing and logically combining a predetermined number of extended address data with received address data.

The examiner fails to show a teaching or suggestion of these limitations in the prior art. Citing page 3, line 23, through page 4, line 6, of the appellants' specification, the examiner asserts that the admitted prior art taught therein "teaches a conversion means responsive to the address data and means for

detecting for logically converting the address so as to prevent the occurrence of the undesired display at an addressable position within the maximum effective display space of the display means." (Examiner's Answer at 4.)

The cited passage of the specification, however, merely teaches that "address data not within the scope of effective address are discriminated ... so that no undesired display can occur within the effective display space." (Spec. at 4.) Neither the production of extended address data or the use of the extended address data to convert address data is disclosed therein. There is no disclosure of therein. Consequently, the passage neither teaches nor would have suggested the hardware conversion means and logic circuit means as claimed.

For the foregoing reasons, the examiner has not established a prima facie case of obviousness. Therefore, we reverse the rejection of claims 1, 3, and 5-8.

CONCLUSION

To summarize, the examiner's rejection of claim 1 under 35 U.S.C. § 112 is reversed. His rejection of claims 1, 3, and 5-8 under 35 U.S.C. § 103 is also reversed.

REVERSED

JERRY SMITH Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)

LLB/dal
NIXON & VANDERHYE
1100 NORTH GLEBE ROAD
8TH FLR.
ARLINGTON, VA 22201